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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,421	09/10/2003	Andrew Strachan	NSC1-M3200 [P05675]	4626

7590 12/16/2005
STALLMAN & POLLOCK LLP
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SAN FRANCISCO, CA 94111

EXAMINER

ISAAC, STANETTA D

ART UNIT	PAPER NUMBER
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2812

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/659,421

Applicant(s)

STRACHAN ET AL.

Examiner

Stanetta D. Isaac

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

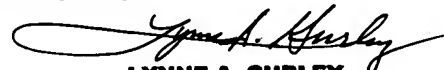
Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 September 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the amendment filed on 8/25/05. Currently, claims 1-3 are pending.

Drawings

The drawings were received on 9/09/05. These drawings are in response to an objection to drawings filed on 2/23/05. The corrections made to the drawings are sufficient to overcome the objection. The objection to the drawings have been withdrawn

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The rejection of claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bol et al., US Patent 6,699,775 in view Pfirsch US Patent 5,736,445 has been maintained for reasons of record.

Bol discloses the semiconductor method substantially as claimed. See figures 1-9, and corresponding text, where Bol shows, pertaining to claim 1, a method of forming a graded junction, in a semiconductor material having a first conductivity type (*Note*: based on the teachings of Bol having the same steps of the method, for example, using a single mask and a single implantation step, it is inherent that a graded junction is formed), the method comprising:

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introducing dopant having a second conductivity type (figure 6B; col. 4, lines 66-67; col. 5, lines 1-5, boron) opposite the first conductivity type into a selected region of the semiconductor material to define a primary dopant region **67, 68, 69** (active regions, pn junction) therein, the perimeter of the primary dopant region defining a primary pn junction (figures 6A-6B; col. 2, lines 5-25; col. 3, lines 63-67; col. 4, lines 60-67; col. 5, lines 1-5); while introducing dopant into the selected region of the semiconductor material, simultaneously introducing dopant into the selected region of the semiconductor material **65, 66** (guard rings) around the perimeter of the primary dopant region and spaced-apart from the primary pn junction (col. 2, lines 27-33; col. 4, 60-67; col. 5, lines 1-5). In addition, pertaining to claim 2, Bol shows a method of forming a graded junction in a semiconductor material having a first conductivity type, the method comprising: forming a patterned mask **22/23/24** on an upper surface of the semiconductor material, the mask including a first opening **62, 63, 64** that exposes a first upper surface area of the semiconductor material and a second opening **60, 61** that defines a perimeter upper surface area that surrounds and is spaced-apart from the first upper surface area (figure 6A-6B; col. 4, lines 60-67; col. 5, lines 1-5); using a single step, utilizing the mask to introduce dopant having a second conductivity type opposite the first conductivity type into the first upper surface area of the semiconductor material to define a primary dopant region **67, 68, 69** therein and into the perimeter upper surface area of the semiconductor material to define a perimeter dopant ring (openings **60** and **61** form the guard rings) therein that is spaced-apart from the primary dopant region thereby defining a primary junction between the primary dopant region and the semiconductor material (figures 6A-6B; col. 2, lines 27-33; col. 4, 45-67; col. 5, lines 1-5). Finally, pertaining to claim 3, Bol shows a method of forming a graded junction in a

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semiconductor material having a first conductivity type, the method comprising: forming a patterned mask 22/23/24 on an upper surface of the semiconductor material, the mask including a first opening 62, 63, 64 that exposes a first upper surface area of the semiconductor material and a second set of openings 60, 61 that define a plurality of quadrilateral upper surface island areas disposed around and spaced-apart from the perimeter to the first upper area (col. 4, lines 1-5, *Note*: since Bol teaches that the desired windows may be segments of closed polygonal or hexagonal annuli it would include island areas); using a single step, utilizing the mask to introduce dopant having a second conductivity type opposite the first conductivity type into the first upper surface area of the semiconductor material to define a primary dopant region therein and into the perimeter upper surface area of the semiconductor material to define a perimeter dopant ring 65, 66 therein that is spaced-apart from the primary dopant region 67, 68, 69 thereby defining a primary junction between the primary dopant region and the semiconductor material (figure 6A-6B; col. 2, lines 27-33; col. 4, 45-67; col. 5, lines 1-5). The primary dopant region and dopant around the perimeter of the primary dopant region are diffused (figure 6C).

However, Bol fails to show, pertaining to claims 1-3, diffusing the dopant in the primary dopant region and the dopant around the perimeter of the primary dopant region to provide a graded dopant region that includes an interior portion that has a first dopant gradient with a first maximum dopant concentration and a perimeter portion that is contiguous with the interior portion and has a second dopant gradient with a second maximum dopant concentration that is less than the first maximum dopant concentration (claims 1-3), and wherein the width of the perimeter dopant ring is less than two times (2x) the lateral diffusion length of the primary junction during the diffusing step (claims 2 and 3).

Pfirsch teaches on figures 1-3b, and corresponding text, a similar method of forming a graded junction in a semiconductor material by using a single mask and reducing the dopant concentration by varying the openings within the mask. In addition, the implanted dopants are diffused laterally beneath the mask regions by a subsequent heat treatment, where the diffusion process is performed in terms of temperature and duration, resulting in regions that are contiguous, providing an improvement in the use of dopant concentration within semiconductor devices (col. 5, lines 3-45; col. 6, lines 2-40 and lines 54-60).

It would have been obvious to one of ordinary skill in the art to, incorporate, diffusing the dopant in the primary dopant region and the dopant around the perimeter of the primary dopant region to provide a graded dopant region that includes an interior portion that has a first gradient with a first maximum dopant concentration and a perimeter portion that is contiguous with the interior portion and has a second dopant gradient with a second maximum dopant concentration that is less than the first maximum dopant concentration, and wherein the width of the perimeter dopant ring is less than two times (2x) the lateral diffusion length of the primary junction during the diffusing step, in the method of Bol, pertaining to claims 1-3, according to the teachings of Pfirsch, with the motivation that an elevation of electric strength can be achieved by varying the openings within the mask in order to vary the dopant concentration. In addition, the diffusion step, taught by Pfirsch, reduces the amount of surface space between transistor devices, resulting in an increase in the number of transistor devices formed on the semiconductor chip.

Response to Arguments

Applicant's arguments filed 8/25/05 have been fully considered but they are not persuasive. In response to Applicant's Remarks, pages 4-5:

Applicant raises the clear issue of whether Bol alone or in combination of Bol in view of Pfirsch, teaches or suggest, a specified width of mask opening.

The Examiner takes to position that the method of forming a graded junction in a semiconductor material having a first conductivity type, as taught by Bol along with the combined teachings of Pfirsch, would lead one of ordinary skill in the art to have a specified width of mask opening. Specifically, Bol shows, in figures 1-2, the use of a single patterned mask that allows for a single implant. It would be obvious that a specified width of the mask opening is obtained based on the fact that a single mask is patterned to include openings, and especially since the Applicant has not disclosed a specified width of the mask opening. In addition, it takes the motivation of Pfirsch that an elevation of electric strength can be achieved by varying the openings within the mask in order to vary to dopant concentration. Furthermore, Pfirsch teaches that the dopant diffuses completely, extending underneath the unexposed portions of the mask, thereby creating a single region. Therefore, it is implied that a lateral dopant gradient profile is performed, since the dopant diffusion region is extended in a lateral direction. Finally, with regards to Applicant's statements of "the guard rings are electrically joined to the main junctions," is a clear issue, however, is not claimed.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

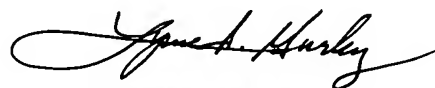
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
December 7, 2005



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